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HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
PARENDO, KEVIN A	

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2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,303	KNECHTEL, ROY	
	Examiner	Art Unit	
	Kevin Parendo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-19 and 21* is/are pending in the application.

4a) Of the above claim(s) *11-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/18/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-9 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "conditioning and premelting of the electrically non-conducting glass paste and the electrically conducting glass paste" on lines 10-11.

The metes and bounds of the claimed limitation can not be determined for the following reasons: neither this claim, nor any dependent claim therefrom, nor the specification, describes in clear detail what "conditioning" refers to. The specification discusses "conditioning" only in paragraphs 19, 29, and 31 of the published application, and does not elaborate other than describing that it is done "in the customary extent and the customary processes". This term is so vague (it is defined by Merriam Webster Dictionary as "to put into a proper state for work or use") that one of ordinary skill in the art would not understand, exactly, the scope of the invention. There are multiple possibilities of what "conditioning" may refer to: (1) forming the glass paste into a specific shape in a specific location; (2) mixing a glass frit with a solvent to form the glass paste, as discussed in Ristic; and (3) stirring the glass paste after it has been formed so that its constituent solvent and glass particles are well mixed. There are

even other possibilities the examiner can imagine ("silver paint" pastes often involve pumping the paste in a vacuum to rid the paste of dissolved air particles, so that they do not form voids when the paste is applied; it is possible that Ristic's conductive frit that has silver adhesive would be similarly conditioned).

If the language of a claim, considered as a whole in light of the specification and given its broadest reasonable interpretation, is such that a person of ordinary skill in the relevant art would read it with more than one reasonable interpretation, then a rejection of the claims under 35 U.S.C. 112, second paragraph, is appropriate. See MPEP 2173.05(a), MPEP 2143.03(I), and MPEP 2173.06. Thus, because this term is not specific and is not defined or discussed in the specification, it is completely necessary for the examiner or a person of ordinary skill in the art to imagine what might be intended by "conditioning", and thus the scope of the claim is unclear.

Claim 1 recites the limitation "conditioning and premelting of the electrically non-conducting glass paste and the electrically conducting glass paste" on lines 10-11.

The metes and bounds of the claimed limitation can not be determined for the following reasons: neither this claim, nor any dependent claim therefrom, nor the specification, describes in clear detail what "premelting" refers to. Because there is no standard definition for "premelting" or "premelt" (for instance, it is not defined by Merriam Webster Dictionary or the Academic Press Dictionary of Science and Technology), one must attempt to guess as to what is meant. Because "pre" means before, the examiner can guess two possibilities: (1) a melting that occurs before some

other event; (2) an event related to a melting process that occurs before melting. The specification only discusses the "premelting" in paragraphs 17, 18, 29, and 31, and none of these discusses what is meant by premelting or what occurs during this process.

If the language of a claim, considered as a whole in light of the specification and given its broadest reasonable interpretation, is such that a person of ordinary skill in the relevant art would read it with more than one reasonable interpretation, then a rejection of the claims under 35 U.S.C. 112, second paragraph, is appropriate. See MPEP 2173.05(a), MPEP 2143.03(I), and MPEP 2173.06. Thus, because this term is not specific and is not defined or discussed in the specification, it is completely necessary for the examiner or a person of ordinary skill in the art to imagine what might be intended by "premelting", and thus the scope of the claim is unclear.

Claims 2-9 and 21 depend from claim 1 and inherit this deficiency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The examination guidelines for determining obviousness under 35 U.S.C. 103 are described in MPEP 2141-2145.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-8, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,094,969 ("Warren") in view of US 5,545,912 ("Ristic") and US 6,817,917 B1 ("Kado").

Re claim 1, Warren discloses a process, wherein at least two processed semiconductor wafers (both **10**'s, see Fig. 2) are located in a middle position of a stack of wafers (the stack consists of both **10**'s and **28**'s, see Fig. 2), and wherein in an operation of a mechanical connecting, electrically insulating connections **24** (column 2, line 68 – column 3, line 3; column 3, lines 63-65; and Figs. 1-2) and electrically conductive connections **25** (column 3, lines 21-24 and 62-63 and Figs. 1-2) are produced between said at least two processed semiconductor wafers each one thereof having a wafer surface side to be connected, said process comprising:

- applying patterned layers (each of 24 and 25 is patterned to cover specific elements, see column 3, lines 1-3, 9, 21, and 39) of an electrically non-conducting paste **24** (column 2, line 68 – column 3, line 1; this is called a "glass frit", which is synonymous with "glass paste" because glass frit are the glass particles which, when screen printed, are dispersed in a solvent, thus

being considered equivalent to a "paste"; for support for this statement, see Ristic, column 2, lines 23-32) and an electrically conducting glass paste **25** (column 3, lines 21-24; also called a "glass frit") on said wafer surface sides (see Fig. 2);

- geometrical alignment of the at least two processed semiconductor wafers to be connected (they are aligned so that the electrical contacts between wafers through the electrically conductive glass exist, see column 3, lines 64-65);
- joining the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the electrically conducting glass paste (they are joined at either 380 degrees or 480 degrees, depending on the specific glass frit used, see column 3, lines 43-49 and 60-65; note, the claimed first and second temperatures need not be different, as the applicant uses them as the same temperature in claim 4) using a mechanical pressure (they are "stacked upon each other to form a sandwiched construction", see column 3, lines 50-52).

Warren does not disclose "processed semiconductor wafers" in the strict definition of wafer (being a semiconductor slab). Warren's wafers are "multi-layered substrates" (column 1, line 15-16) being a ceramic circuit board (column 1, lines 44-46

and 58-60). However, it is well known to store ICs and other devices between processed semiconductor wafers.

For example, Ristic discloses (see Figs. 1-2) bonding semiconductor substrate **12** (column 2, lines 12-13) to semiconductor cap **16** (column 2, lines 15-16 and column 3, lines 21-24) using insulating or conducting glass frit **14** (column 2, lines 23-32 and column 3, lines 41-48) so that devices **26** (column 2, line 15) are enclosed in cavities **18** (column 2, line 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Ristic to the invention of Warren.

The motivation to do so is that the combination produces the predictable results of bonding not only ICs but other devices (such as 26), in a situation where conductive substrates (column 2, lines 12-13 and 15-16) may be joined so that electrical connections between them may be made (column 3, lines 18-14 and 44-48). This is useful for specific device types, such as accelerometers (column 3, line 64) or transistors, resistors, capacitors, inductors, transducers, or surface acoustic wave devices (column 5, lines 30-32) that may require hermetic sealing (column 2, line 18) in a cavity to provide EMI shielding (column 5, lines 44-46).

Thus, herein, when "semiconductor wafers" is discussed in terms of Warren, it is to be understood that the semiconducting materials of Ristic are being substituted for the ceramic circuit boards. This avoids the need for repetition of the above paragraph.

Warren does not explicitly disclose "conditioning and premelting of the electrically non-conducting glass pastes and the electrically conducting glass paste". However, the examiner notes the rejection of the claims under the second paragraph of 112, above, for the ambiguity of the "conditioning" limitation. The examiner notes that the conditioning is disclosed by the Applicant to be "customary" (paragraph 19 of the published application). It is therefore an obvious condition for one of ordinary skill in the art to apply. Also, for example, the mixing of the glass frit and solvent together to form the paste (Ristic, column 2, lines 23-32) can be considered "conditioning". Warren's mixing in the silver adhesive (column 3, lines 17-20) only in the conducting paste may be interpreted as "conditioning" that is different than the "conditioning" of the non-conducting paste. Thus, the "conditioning" limitation would be obvious to one of ordinary skill in the art.

Regarding the "premelting", Kado discloses "pre-baking" glass frit at 350 degrees (column 7, lines 45-49 and column 16, lines 16-21). This is interpreted as "premelting" because it is a heating process conducted before the melting.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kado to the invention of Warren and Ristic.

The motivation to do so is that the combination produces the predictable results of heating the glass paste so that resin and other materials are removed (column 7, lines 45-49 and column 16, lines 16-21).

Re claim 2, Warren further discloses that the electrically non-conducting glass paste and the electrically conducting glass paste are applied by a screen printing process (column 3, line 39).

Re claim 3, Warren and Ristic disclose the limitations of claim 1, as discussed above. Neither Warren or Ristic further discloses that the electrically non-conducting glass paste and the electrically conducting glass paste have different conditioning conditions and premelting conditions and, therefore, the conditioning and the premelting are implemented successively, each in a separate conditioning and premelting process.

The examiner notes the rejection of the claims under the second paragraph of 112, above, for the ambiguity of the "conditioning" limitation. The examiner notes that the conditioning is disclosed by the Applicant to be "customary" (paragraph 19 of the published application). It is therefore an obvious process for one of ordinary skill in the art to perform. For example, the mixing of the glass frit and solvent together to form the paste (Ristic, column 2, lines 23-32) can be considered "conditioning". And this, together with Warren's mixing in the silver adhesive (column 3, lines 17-20) only in the conducting paste may be interpreted as "conditioning" that is different than the "conditioning" of the non-conducting paste.

Regarding the "premelting", the examiner notes the ambiguity regarding this term, as discussed above with the 112 rejection. Kado discloses "pre-baking" glass frit at 350 degrees (column 7, lines 45-49 and column 16, lines 16-21). This is interpreted as “premelting” because it is a heating process conducted before the melting. It also

appears to be a well known process that is part of a general "conditioning" that occurs while using glass pastes in the prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Kado to the invention of Warren and Ristic.

The motivation to do so is that the combination produces the predictable results of heating the glass paste so that resin and other materials are removed (column 7, lines 45-49 and column 16, lines 16-21).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a process such that the electrically non-conducting glass paste and the electrically conducting glass paste have different conditioning conditions and premelting conditions (since Warren adds silver adhesive to the areas that are conductive, the conductive portion would have different physical properties and thus different conditioning and premelting properties) and, therefore, the conditioning process and the premelting process are implemented successively, each in a separate conditioning and premelting process (if they both have different conditions, it is necessary to perform them successively, because it would not be possible to perform them simultaneously).

Re claims 4 and 5, Warren does not disclose explicitly that

- that the first processing temperature of the electrically non-conducting glass paste and the second processing temperature of the electrically

conducting glass paste are "the same processing temperature" (**claim 4**); or that

- the first processing temperature of the electrically non-conducting glass paste and the second processing temperature of the electrically conducting glass paste are "different processing temperatures" and wherein the first processing temperature and the second processing temperature are successively passed in the process of joining the at least two processed semiconductor wafers (**claim 5**).

Rather, Warren discloses that both **24** and **25** are heated to either 380 or 480 degrees, depending on which type of glass frit is used (see column 3, lines 44-47). Thus, both **24** and **25** are made of the same glass frit. They then have the same "processing temperature" if it is interpreted as the temperature at which both frits are heated to and that is sufficient to melt both frits. This thus renders claim 4 unpatentable.

The non-conductive frit is made to be conductive by adding silver/glass conducting adhesive (see column 3, lines 17-20) in specific areas where conductive frit is desired. If "processing temperature" is interpreted as a "melting temperature", then one of ordinary skill in the art at the time of invention would understand that since the frits began as the same, with the same melting temperature, that adding another adhesive composition to the frit to make it conductive would alter its physical properties including its melting temperature. Thus, they would have "different processing temperatures". Warren then heats to a higher processing temperature (e.g. 480) that is

sufficient to melt both frits. Warren thus would have to successively pass both melting temperatures by during the connecting/joining.

Re claim 6, Warren further discloses that at least one of the at least two processed semiconductor wafers has an electrical connection in an area that does not contain electronic structures (see column 3, lines 21-24, wherein the substrates are connected electrically, but not the ICs).

Re claim 7, Warren further discloses that the at least two processed semiconductor wafers are electrically connected at specific electric circuit points in areas containing electronic structures (see column 1, line 64 - column 2, line 5, wherein "the ICs may be electrically connected between the stacked boards").

Re claim 8, Warren further discloses that the joining of the at least two processed semiconductor wafers further comprises the first processing temperature and the second processing temperature being about 450°C (they are joined at either 380 degrees or 480 degrees, depending on the specific glass frit used, see column 3, lines 43-49 and 60-65).

Re claim 21, Warren further discloses that the applying of the patterned layers comprises applying a first patterned layer of the electrically non-conducting glass paste to the wafer surface side of a first one of the at least two processed semiconductor

wafers (see column 1, lines 63-65, wherein the non-conducting glass frit is formed to cover "each individual" wafer; see column 2, line 67 – column 3, line 3, wherein the ICs **20** may be covered, but only one of which is shown; thus, both sides of each **10** are covered with **24**) and applying a second patterned layer of the electrically conducting glass paste on the wafer surface side of a second one of the at least two processed semiconductor wafers (when **25** is made to be conductive in some selected area, is necessarily is either on the top or bottom of a wafer **10**; thus, there will be **24** on one side of one wafer **10**, and there will be **25** on the opposite side of an adjacent wafer **10**).

3. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Warren, Ristic, and Kado, as applied to claim 1, above, and further in view of US 2003/0170936 A1 ("Christensen").

Re claim 9, Warren, Ristic, and Kado disclose the limitations of claim 1, as discussed above, but fail to further disclose that one of the at least two processed semiconductor wafers is a SOI wafer comprising an active semiconductor layer and a buried oxide layer on a substrate and wherein an electrical connection to the substrate of the SOI wafer is implemented through previously produced openings in the buried oxide layer and in the active semiconductor layer.

Christensen discloses that one of the at least two processed semiconductor wafers is a SOI wafer (paragraph 2) comprising an active semiconductor layer and a buried oxide layer **106** or **108** (paragraph 20) on a substrate **104** (paragraph 20) and wherein an electrical connection to the substrate of the SOI wafer is implemented

through previously produced openings **300** (Fig. 3 and paragraph 24) in the buried oxide layer **106 or 108** (Fig. 3) and in the active semiconductor layer **102** (Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Christensen to the invention of Warren, Ristic, and Kado.

The motivation to do so is that the combination produces the predictable results of connecting a SOI wafer with improved speed of signals (paragraph 2) to an external wafer.

Response to Arguments

4. Applicant's arguments with respect to claims 1-9 and 21 have been considered but are not persuasive.

5. Regarding the 112 rejections to claim 1, the applicants argue that "one of ordinary skill in the art would appreciate that in preparing layers of glass paste containing glass particles and an organic solve, as require by claim 1, after completion of mixing the constituents of the glass paste, printing a layer on the substrate, the following steps may take place". They then point to "Ferro" and to "Masuko" as evidence of a drying and of a binder burnout. (See remarks, page 8). This is unpersuasive, as claim 1 does not require "preparing layers of glass paste containing glass particles and an organic solve". Neither do claims 2-9 or 21. Neither is this described in the specification. In fact, the claim discusses "patterned layer of an electrically non-conducting glass paste and an electrically conducting glass paste", and

the specification discusses "glass" (paragraph 16 of the published application) "glass paste" (paragraph 16), "glass frit" (paragraph 9), and "glass solders **6**, **5**" (paragraphs 17 and 24). Because the specification describes multiple materials, none of which involves the "glass particles and organic solve", this argument is unpersuasive.

6. Further regarding the 112 rejections to claim 1, the applicants argue that "the premelting step is defined in the present disclosure. See, e.g., present disclosure, paragraph [0028]" (see page 8). This is not persuasive, as paragraph 28 of the published application refers to "screen printing". Sometimes the paragraphs are different by one or two between the application as filed and the published version - paragraph 29 describes "conditioning and premelting of the electrically non-conducting glass paste" and paragraph 31 describes "conditioning and premelting of the electrically conducting glass paste". Neither of these does anything other than cite the term "premelting" – there is no "definition" or even any example of one instance of what "premelting" may mean.

7. The examiner has withdrawn the 112 rejection to claim 8, as it is deemed that one of ordinary skill in the art would take "in a range of 450" to mean "being about 450", as the claim has been amended to read.

8. Regarding the 103 rejections, the applicants argue in multiple instances limitations that are not claimed. It is noted that, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For example, applicants argue that "the cover 16 of Ristic cannot be interpreted as a processed wafer because cover 16 does not contain any circuitry. Because there is no circuitry in the cover 16, no circuitry can be connected to any circuitry located on substrate 12 of Ristic" (see pages 11-12). This is unpersuasive, because there is no claimed limitation in claim 1 that requires the "processed wafer" to contain circuitry. There is no claimed limitation in claim 1 that requires such circuitry to connect to circuitry in substrate 12. The term "processed wafer" is generic and merely involves "processing", which can be forming semiconductors or passive components in a wafer, or merely cleaning or etching a wafer, or coating a wafer. Applicants further argue that "an embodiment of the present disclosure is directed to... joining the two wafers with their respective layers in a final processing step which not only joins the two wafers by bonding but also completes the electrical circuitry contained on the two processed wafers" (see page 12). Again, the pertinent issue to discuss is the claimed invention, not an embodiment of the disclosure. Claim 1 does not require the joining of the wafer in "a final processing step", nor does it require "complet[ing] the electrical circuitry contained on the two processed wafers".

Arguments regarding the dependent claims 2-8 (see page 12, 3rd paragraph) merely point back to the arguments just discussed. Arguments regarding the dependent claim 9 (see pages 12-13) merely point back to the arguments just discussed.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicants' amendments were made to overcome the examiner's objections, using the examiner's suggestions word-for-word in many instances. The rejections above are only changed to indicate these changes. The overall grounds for rejection have not been changed. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Parendo, whose can be contacted by phone at (571) 270-5030 or directly by fax at (571) 270-6030. The examiner can normally be reached on Mon.-Thurs. and alternate Fridays from 7 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin A. Parendo/
Examiner, Art Unit 2823
1/13/2011

/Hsien-ming Lee/
Primary Examiner, Art Unit 2823